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# Recent Research Trends in Thin Film Solar Cells

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**Abstract:** A brief review of the scientific status of thin film solar cells is presented, and the generic research challenges identified. A study of the control of grain size in the sublimation growth of CdTe is described in which the pressure of an ambient gas was used to control the nucleation density and hence grain size. Grain diameter varied with pressure according to $D$ (μm) = 0.027 (±0.011) x $P$ (torr) + 0.90 (±0.31) for pressures up to 200 torr. It was found that PV devices made using large-grained CdTe increased in efficiency up to the point where the grain boundary resistances were no longer limiting. The electrical performance of CdS/ITO and CdS/$SnO_2$ junctions were investigated for both as-grown and oxygen annealed CdS surfaces. The latter induced rectification, regardless of the substrate type, this being attributed to the formation of a CdO/CdS junction. Attempts to influence the performance of CdTe/CdS devices grown on oxidized and reduced CdS are described.

**Key words:** Solar photovoltaic, CdTe, CdS, grain boundaries.

The purpose of this paper is to review key aspects of the scientific status of a range of solar photovoltaic (PV) technologies, to identify some general themes and challenges, and to report progress in two key areas for CdTe/CdS solar cells, these being grain control and transparent conductors.

It is well known that solar energy has vast potential for power generation. Moreover, the rate of increase in the solar PV generating capacity worldwide continues to increase. At present, the current position is regularly updated on the website of the European Photovoltaic Industries Association (Anonymous, 2010). Presently the rate of increase in deployment exceeds 50% per annum, the world leader being Germany. That country's success and position is due to several decades of investment in research and development and, more recently, support for new industry in the form of a feed-in tariff. This regulatory tool encourages domestic level investment in PV by imposing a lucrative buy-back price to be paid by generating companies for solar electricity – this encourages and stimulates the market. From a scientific standpoint the objective is to improve the PV materials and devices to the point at which they generate power that is genuinely competitive with grid connected power.

In 2010, the PV market worldwide is dominated at the level of 90% by single crystal and polycrystalline silicon, this percentage having fallen by 5% in a few years. This change is due to the emergence of thin film PV as a major emerging market force. In particular, CdTe has become the manufacturing technology of the World's number two manufacturer of PV, First Solar Inc. There are a number of emerging technologies and it is tempting to attempt to predict the 'winner', that will be dominant in the market in perhaps 20 years time. Criteria might include price, stability, sustainability, and ease and suitability of deployment for example. However, there is no clear future leader at the present time. For example, even though the thin film technologies are fundamentally cheaper, the costs of silicon PV manufacturing are conforming to a 'learning curve' pattern, and continue to decrease.

It is nevertheless an exercise to evaluate the scientific and technological status of some key PV technologies. The assessment that follows is a brief and non-exhaustive survey.

(a) Bulk single crystal silicon presents a highly engineered PV solution with laboratory efficiencies approaching the fundamental limit, and being close to 25%. It is the superb control of silicon that has allowed production efficiencies to reach 23% with the Sanyo HIT cell.

(b) Bulk polycrystalline silicon enjoys a cost advantage over single crystal silicon. However, it has an inherent processing disadvantage in that each surface crystallographic orientation will have a slightly different response to

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processing, leading to overall lowered efficiency, the best at present being ~20%.

(c) Thin film silicon is attractive as an alternative to bulk silicon, since its use would capitalize on the corpus of knowledge open to the bulk material itself. The disadvantage is that silicon is an indirect band gap material, and as such is a relatively weak absorber. Hence in order to use thin film silicon effectively, strategies for enhanced light capture and utilization need to be established. The first of these was the deployment of amorphous silicon, which has a direct gap, and this was pioneered as the University of Dundee in the UK (Spear and Lecomber, 1975). Despite becoming a major international product (remaining very actively in production), amorphous silicon suffers the disadvantage of low efficiency (~6%) and photo-instability via the Stabler Wronski effect (Staebler and Wronski, 1980). Other, crystalline, forms of silicon, suffer from their indirect band gap and low in absorption as mentioned above. Strategies to overcome this are (i) coupling of amorphous and micro-crystalline thin film silicon into a tandem cell - the band gaps of 1.7 and 1.1 eV make this ~8-9% efficient, and it is in production, (ii) use of metal nanostructures to achieve coupling of energy from plasmon resonance into the p-n or p-i-n junction, and (iii) use of light scattering structures to increase the path length of light in the absorber. It may be anticipated that thin film silicon will become an important product if the problem of its low absorption can be overcome using this or other methods.

(d) Work on CdTe/CdS solar cells dates back to the 1970s and continues to evolve by R&D effort and in production. Its advantage is in the high absorption coefficient of CdTe, which is approximately 100 times that of silicon. This is a polycrystalline technology with low cost doping and processing, and this has required substantial research effort to generate product that is robust to processing in the industrial environment. There have been particular challenges in doping, contacting, and the role of interfaces, especially grain boundaries, interdiffusion, and contacts. Overall though, CdTe is tolerant of many processing variables, possibly on account of its near-stoichometric vapor growth behavior. At the time of writing, First Solar Inc. are manufacturing almost $1GW_p$ (giga Watt peak) of generating capacity, making CdTe a spectacular success in the market. Cd is known to be toxic, but in the form of CdTe it is very stable, making the modules themselves low-risk, particularly if returned for re-cycling. The Cd issue is addressed by Fthenakis (Fthenakis, 2004).

(e) $Cu(In,Ga)Se_2$ ('CIGS') is an alloy of $CuInSe_2$ and $CuGaSe_2$ with a closer to optimum band gap than either of the constituents. It is a direct gap polycrystalline absorber, and in the lab it performs at higher record levels than does CdTe (19.2% (Contreras *et al.*, 2006 compared to 16.5% (Wu, 2004). Arguably this is due to the ability to adapt the processing in CIGS to take advantage of the broad spectrum of vacancy and substitutional doping opportunities. At the present time, while there are many small and medium sized companies producing CIGS and related chalcopyrites, there is no giant. This may be related to the complexity of the material itself, but time will tell.

(f) Future technologies are under investigation, and there is an increasing shift towards sustainable, low cost semiconductors based on abundant elements. A key and emerging example is based on the kesterite family of materials, for example $Cu_2ZnSnS_4$. This, and its analogues with Se and Te, may be understood in terms of substitution of expensive In with the isoelectronic combination of Zn and Sn. The family of materials is becoming increasingly popular as a subject for research (see for example Katagiri *et al.*, 2010).

Generally, the thin film PV technologies are limited by the level of understanding of the materials themselves, and the related control issues. The origin of this can be traced back to the paradigm for thin film solar cells developed in the 1970s: the philosophy was to immediately fabricate PV junctions based on ideal heterojunction partners. To reduce the cost, it was postulated that low purity polycrystalline layers could be deposited in which the correct electronic structures (fields) could be encouraged by post-deposition processing, e.g. by heat treatment. While this empirical approach initially led to rapid developments, it generated some blind alleys in research, notably the $Cu_xS/CdS$ junction that later proved to be unstable to diffusion effects. Perhaps controversially, progress in the technologies that are successful today has been achieved by back-tracking from this approach in order to identify the efficiency limiting aspects of each device technology. Generally following are the critical materials issues are:

*Conductivity control of the semiconductors*

Conventionally this would be achieved by impurity doping, for example n-doping of Si being achieved by $P_{Si}$, p- by $B_{Si}$, with the desired profiles being controlled by diffusion. However, in the thin film methodology, conductivity type is manipulated using the basic properties of the semiconductor materials themselves. For example, CdS is 'naturally' easy to make n-type since heating it encourages loss of S and hence creation of $V_S$ donors. Unfortunately such doping is not always so simply achieved, and the most successful processing procedures are sometimes complex and apparently contrary. In the case of CdTe, the intention is to create a p-type partner for CdTe, and this is achieved partly by the use of Cl doping. Although $Cl_{Te}$ is expected to act as a donor, it is thought that in solar cells its combination with the double acceptor $V_{Cd}$ is responsible for the single acceptor complex 'A-centre', [$Cl_{Te}$-$V_{Cd}$]. This processing is universal in CdTe solar cell manufacture, even though it relies on complex interactions and probably on competing diffusion fronts that are difficult to control. In order to gain more full control over the doping profile, there is limited research on fabrication of intentionally doped MOCVD-grown CdTe solar cells. This has been most successful using co-doping with As and Cl. This approach was arrived at empirically and although it has yielded dot cell results with efficiencies up to ~13% (Irvine *et al.*, 2008), there is much that is not understood about the in-gap defect levels. This is under investigation by thermal admittance spectroscopy (Barrioz *et al.*, 2005).

*Grain boundaries*

Thin film solar cells grown on cheap amorphous substrates (glass) are by their very nature polycrystalline. Grain boundaries are generally understood to be deleterious to solar cell operation for a number of reasons including; (i) the distribution of orientations presented to the surface makes processing non-uniform, (ii) the boundaries may act as barriers to current transport, (iii) the boundaries may promote minority carrier recombination, and (iv) the boundaries may encourage accelerated diffusion leading to complexities in the process control, and a mechanism for degradation of the cell performance with time. As a result, much effort has been made on controlling grain boundaries, and characterizing their influence in solar cell devices. For example in thin film silicon, it has been demonstrated that large grains can be grown at low temperatures on glass substrates by the use of an aluminium induced recrystallisation step. The procedure is to deposit aluminium layers on glass and to overcoat this with small-grained silicon. Annealing induces the formation of a low temperature eutectic, which promotes recrystallisation. Following this the aluminium is segregated to the surface where it can be etched off, leaving a large-grained template layer for epitaxial thickening. A second example is for CIGS, in which accidental contamination with sodium (from glass substrates) encourages the formation of a {112} preferred orientation and larger grains than usual.

*The role of important device layers and interfaces*

In modern thin film solar cells, the transparent conducting electrode is a critical component – for a wide range of technologies. Usually this is a multi-layer of transparent conducting oxides, or TCOs. It has been recognized for some years that the TCO plays more than a passive role in device operation. It has been recognized that increasing the thickness of indium tin oxide in CdTe/CdS solar cells caused a gradual increase in the fill factor, but that this plateaued, presumably when the resistance of the TCO was no longer limiting in those devices. This result clearly indicated the importance of the TCO having a sufficiently high conductivity. More generally it has been seen in a variety of devices that inclusion of a nominally resistive layer between the TCO and the semiconductors increases the device performance. This has been observed in thin film silicon (von Roedern and Bauer, 1999), CdTe (Irvine *et al.*, 2008) and CIGS (Kanevce and Sites, 2007). This layer is sometimes referred to as 'high resistive transparent' or HRT layer, although it might more accurately be named a 'voltage protection layer'. The mechanism is the subject of several theories, which are not exclusive – these are reviewed briefly for the case of ZnO being the capping layer for a TCO for use with CdS:

(i) if it is postulated that current leakage paths act to partly short the junction, then it is feasible that the spatial extent of the influence of such 'pinholes' may be limited by the inclusion of a resistive sheet. This has been the subject of a resistor network model (Kanevce and Sites, 2007), which indicates that such a layer would indeed have a beneficial effect, and

(ii) the extra layer may influence the interface states or band line-ups at the CdS/TCO interface in a beneficial way. Evidence to support the latter comes from the observation, by impedance analysis, that under illumination the layer does not act as a limiting resistance in the solar cells (Proskuryakov *et al.*, 2009).

Further to this, the TCO is implicated in CdTe/CdS as having a potentially complex interaction with the processing of the layers deposited upon it. In particular, post-growth processing of CdS by annealing in air is sometimes used as an intermediate step to influence the properties of full devices. Alamari and Brinkman (2000) have shown that it may sometimes lead to the formation of a junction that is electrically in opposition to that of the main p-n junction – clearly this situation would not help the formation of high efficiency devices.

In this paper, some recent findings on grain size control, the effects of oxygen annealing of CdS, and their influence on devices are presented.

## Experimental

### *Influence of CdTe grain size on cell performance*

CdTe growth studies were undertaken in specially designed close space sublimation (CSS) apparatus built by Electro-Gas Systems Ltd, UK. 5N purity CdTe was sublimed from a 5 x 5 $cm^2$ source tray onto substrates comprising CSS CdS on Pilkington TEC15 glass. In a series of growth runs, the grain size was evaluated after growth under pressures of $N_2$ varied in the range 2 – 200 torr. In each case the growth time was adjusted to give layers of constant thickness (~6 μm). The layers were fabricated into PV devices by annealing with $CdCl_2$ and contacting with gold – the procedures are described by Major *et al.* (2010). The current-voltage (J-V) behavior of the cells was evaluated under simulated AM1.5 radiation at approximately 1000 $W.m^{-2}$.

### *Processing CdS/$SnO_2$ and CdS/ITO by annealing.*

CdS layers were grown by CSS onto both $SnO_2$/glass (Pilkington TEC15) and ITO/glass (Delta Technology) substrates. The layers were examined in their as-grown states and after annealing under 100 torr of oxygen for up to 40 mins at 400°C. The electrical response of the CdS/TCO junctions was evaluated by contacting the CdS with In, which is generally thought of as Ohmic. However, since the CdS layers are 200-400 nm thick, and prone to pinholing, their electrical integrity was checked by the use of gold dots. Gold is expected to form a rectifying contact to CdS. Hence if an Au/CdS/TCO structure showed rectifying behavior, then the CdS layer may be considered to be pinhole free. In practice, each In dot studied was checked by surrounding it with four gold dots. The layers were also evaluated by grazing incidence XRD and Auger electron spectroscopy to check for the development of oxides. In order to check the influence of post-growth treatment of the CdS on device performance, devices were fabricated on layers that had been annealed with $O_2$, $H_2$ and $N_2$ containing ambients at 400°C for 4 mins. In this case the CdS was deposited by chemical bath deposition at Cranfield University. The cells were completed by CSS deposition of CdTe and using the procedures described in Major *et al.* (2010).

## Results and Discussion

### *Influence of CdTe grain size on cell performance*

Varying the pressure of $N_2$ present in the chamber during the growth of CdTe by CSS had a profound influence on the grain size of the layers, as shown in the scanning electron micrographs shown in Fig. 1. There is a clear increase in grain size with pressure. Grain size distribution data was extracted from the images – it was found that the average grain size increased linearly with $N_2$ pressure according to the relation $D$ (μm) = 0.027 (±0.011) x $P$ (torr) + 0.90 (±0.31).

This result may be understood in terms of the factors that influence the formation of stable nuclei on the surface of a film, and the relationship between such nuclei and the grains that are present in the final film. By analogy with the case for 3D precipitation, free energy considerations indicate that a nucleus on a surface may only become stable if it exceeds a critical radius. Such nuclei form by the processes of aggregation of atoms at a point, following surface migration and direct impingement on the nucleus point itself. Clearly if the impingement rate of gas species at the surface is high, then the density of nuclei that formed is also likely to be high. In the presence

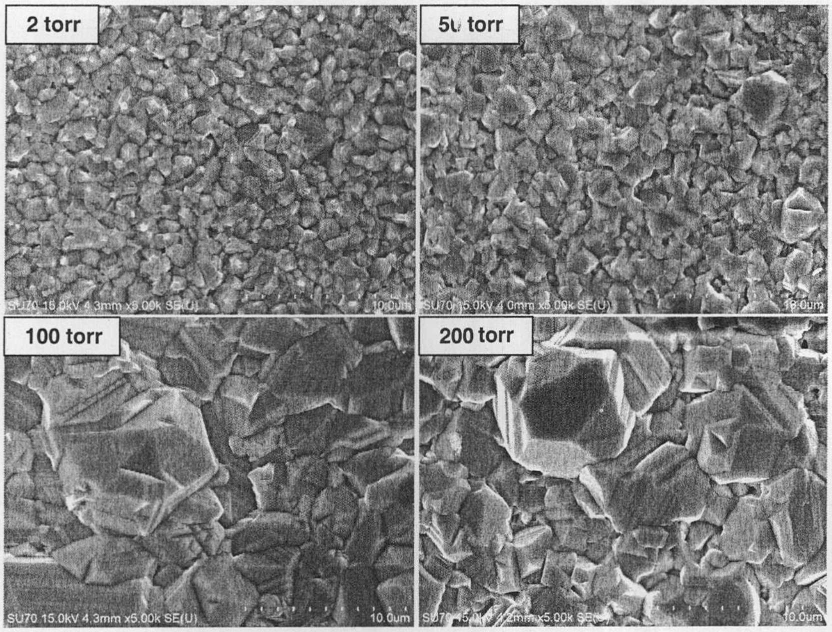


*Fig. 1. Scanning electron micrographs of CdTe grains in films grown by CSS under pressures of $N_2$ in the range 2 - 200 torr. Analysis of the grain size distributions indicated a linear relationship between the average grain size and thickness h, according to D (ìm) = 0.027( 0.011) x P (torr) + 0.90( 0.31).*

of a high pressure of inert gas, the arrival rate of atoms at the surface is reduced, and hence the nucleation density is correspondingly reduced. Since each stable nucleus may be considered to expand to form a single grain in the completed film, it follows that at higher pressures, the nucleation density will be lower, and larger grains will result.

The working parameters for devices made from similar layers are shown in Fig. 2. There is a clear increase in the *Voc*, *Jsc*, *FF* and efficiency with pressure (grain size) up to a maximum limit (100 torr) after which there is a plateau in performance. Much of this increase may be attributed to the decrease in the series resistance (*Rs*) of the cells associated with the increase in grain size. For the cells shown, *Rs* was 700, 180, 50 and 20 Ω, respectively. This may be understood in terms of the grain boundaries being resistive in the devices, particularly when they are oriented parallel to the junction, in which case the carriers must cross them in order to flow through the cell. The appearance of a plateau (Fig. 2) may be the result of the grains reaching such a size as to no longer be the limiting resistance in the cell. For example, when the grain diameters exceed the film thickness, it may be expected that there are only vertical grain boundaries in the film, and none that contribute to the perpendicular resistance.

## *Processing CdS/$SnO_2$ and CdS/ITO by annealing*

The use of gold contacts to test for the integrity of the CdS films proved to be a sensitive method of detecting pinholes. For films grown by sublimation methods, it was possible to detect growth conditions and edge effects that lead to the formation of films with pinholes leading to Ohmic behavior, even though Au/CdS junctions are expected to be rectifying. Furthermore, ITO supplied by certain manufacturers was found to encourage the formation of shorts more than that from others. The combination of CBD CdS grown on Delta Technology ITO was found to give reliable results. Nevertheless, for the In/CdS/TCO dots studied in this work, each one was surrounded by four Au dots and it was verified that shunting was unlikely to interfere with the results in these samples.

For all samples of both the In/CdS/ITO and In/CdS/ITO types studied, it was found that for as-grown CdS they were Ohmic in all cases. However, for the case of CdS, which was annealed and then contacted with indium, the samples always displayed rectifying behavior, as shown in Fig. 3. Since this property was independent of the type of TCO used, it was considered a property of the CdS, not the TCO, and hence the surface chemistry of the CdS was investigated

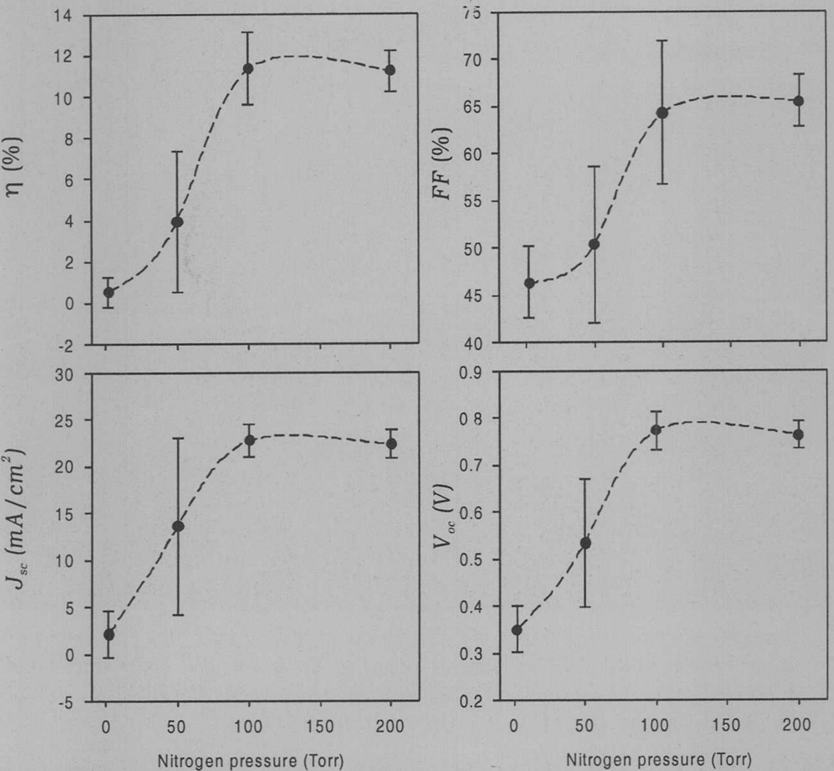


*Fig. 2. Working parameters of CdTe/CdS solar cells fabricated from CdTe layers having progressively larger grain sizes. The performance reaches a plateau when the grain boundaries cease to be limiting, as desc.ibed in the text.*

by x-ray diffraction and Auger electron spectroscopy. Grazing incidence XRD revealed no extra phases, indicating that there is either none present (below the detection limit) or else are

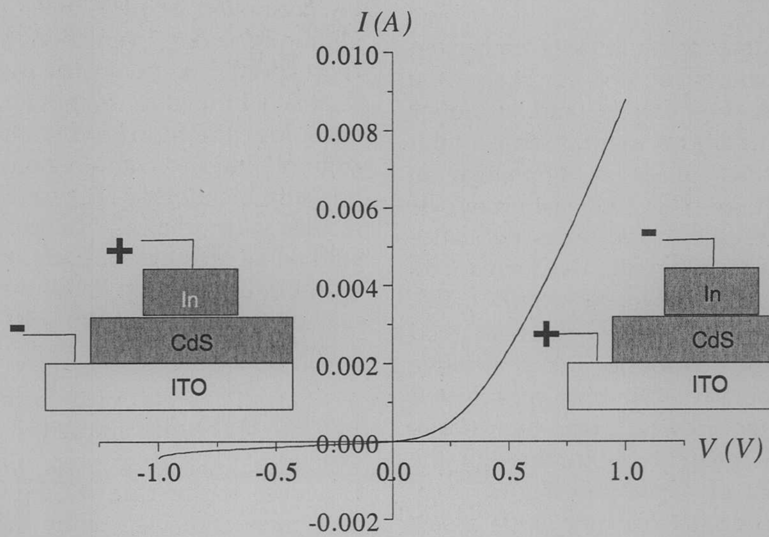


*Fig. 3. I - V curve for the In/CdS/ITO junction obtained from a sample for which the CdS had been annealed in oxygen before application of the In contact. I – V curves from In/CdS/SnO2 were similar (i.e. rectifying) while those obtained from both samples in their as-grown state showed no rectification and were Ohmic.*

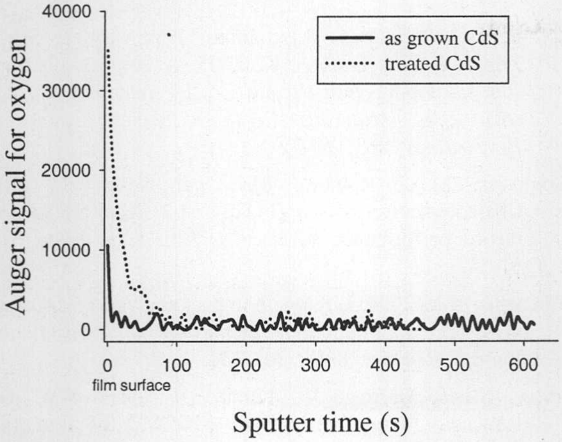


*Fig. 4. Auger depth profiles for oxygen in CdS for both as-grown surfaces and a sample that had been heated in oxygen. The heat treatment has clearly increased the concentration of oxygen near the surface, and this is consistent with the formation of CdO.*

amorphous. On the contrary, the Auger depth profiling results show that annealing increases the concentration of oxygen at the surface of the CdS, and it may be inferred that there is an overlayer of CdO.

In order to test whether this is consistent with the rectifying results, a band diagram for In/CdO/CdS/ITO was constructed using published data for the band gaps ($E_g$), electron affinities and work functions of the relevant materials, as shown in Fig. 5. The proposed band structure shows the presence of a field at the CdO/CdS junction that is of the correct sense to account for the rectification of results observed. These results support the hypothesis that the rectification is a property of the CdS rather than of the underlying TCO. Earlier pioneering work in which differences in the behavior of ITO and $SnO_2$ based devices were reported (Alamari and Brinkman, 2000) may have been influenced by undetected pinholes.

The devices fabricated with CdS that had been post-growth annealed in $O_2$. $H_2$ and $N_2$ were intended to reveal whether such annealing had a deleterious, or perhaps beneficial effect on the performance of solar cells. Hence the conditions used to fabricate the cells were chosen for reproducibility rather than the highest performance. Typically the devices had comparable performance, irrespective of the annealing treatment used, with the working parameters being $\eta$ = 6.5%, *FF* = 53%, *Jsc* = 19 mA.cm$^{-2}$ and *Voc* = 0.61 V for samples contacted with 2 mm diameter gold dots. An explanation for the failure of annealing (in either reducing or oxidizing ambients) to change the device performance may be that the overgrowth with CdTe acts to reverse, or else normalize, the effects of annealing. This is likely since while the annealing was done at ~300°C in each case, the CdTe growth was at ~300°C. It remains possible that annealing in more extreme oxidizing or reducing conditions may have an effect on devices.

## Conclusions

The PV market continues to increase, partly driven by government subsidies that are designed

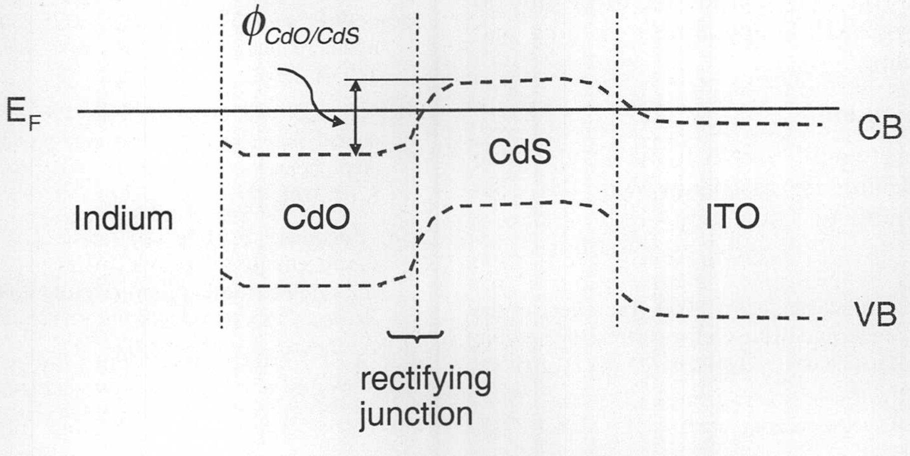


*Fig. 5. Proposed band structure for the In/CdO/CdS/ITO structure. The sense of the field at the CdO/CdS junction is opposite to that in the CdTe/CdS junction and therefore the formation of CdO on CdS is expected to be harmful to device performance.*

to stimulate PV manufacture and the related industries. It is the objective of scientific research to increase the efficiency and to make PV cost effectiveness to the point at which it is able to generate power in competition with that from fossil fuels.

Presently, the thin film technologies, notably CdTe, are becoming commercially important. Generic issues for thin film research include grain control, doping and impurity control, and the understanding of electronic and optical structures. Continued effort on these topics is necessary to not only improve competitiveness, but to reduce the technological risk for manufacturers.

In this paper, the control of grain size in CdTe was demonstrated. It was achieved by using gas pressure in the sublimation chamber to reduce the nucleation density and hence to increase the grain size in completed films. Devices made from a series of films with increasing grain size showed increased performance parameters up to a plateau, above which the grain boundary resistances were presumed to be no longer limiting. In the second study presented here, oxygen annealing of CdS on both ITO and $SnO_2$ coated glass substrates was re-visited. It was found that such annealing caused test structures (In/CdS/TCO) to become rectifying for both kinds of substrate, whereas the as-grown materials were always Ohmic. In order to achieve reliable results, care was taken to work with samples, which were pinhole-free. The result was ascribed to the formation of CdO. However, neither oxidation nor reduction of CdS used in complete devices caused a change to the device performance. This was considered to be due to the CdTe overgrowth temperature exceeding that of the annealing.

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